



OVERVIEW: Hands-On-Training Experience in VLSI Design

1. Digital Electronics:

- a. Introduction to VLSI design
- b. Basics of Digital Electronics
- c. Combinational circuit design concepts
- d. Sequential circuit design concepts
- e. Introduction to Finite State Machine.

2. Verilog HDL

- a. Hardware Modeling Overview,
- b. Verilog language concepts
- c. Introduction to Testbenches
- d. Operators
- e. Dataflow
- f. Procedural Statements
- g. Finite State Machines

3. Lattice Diamond:

- a. Implementation Flow
- b. Synthesis
- c. Pin constraints
- d. Timing Simulation using Active HDL
- e. Configuration

4. FPGA Architecture:

- a. FPGA fundamental concepts
- b. Study of Lattice FPGA
- c. FPGA design flow

5. Application includes

- a. Half Adder
- b. Full Adder
- c. Simple Up/Down Counter
- d. BCD Up/Down Counter
- e. Flip Flops.
- f. Drive a LED
- g. Timing a LED
- h. 7-Segment display
- i. Counter using 7-Segment Display
- j. Push button
- k. Pulse Width Modulation

Note:-

1. Course fee is Rs 8000 + 10.3% tax = Rs 8824 (including registration, training, Reference CD)
2. Students will receive certificates from EFY Enterprises on successful completion of class in VLSI Design.
3. At the end of the course a CD will be provided with the information about Reference manual, Data manual and necessary details.